IN THE CLAIMS

1. (Currently Amended) A method of defining a feature on a substrate, comprising:

(a) providing a substrate having a multilayer stack formed thereon;

(b) forming a first mask ~~through~~ by patterning one or more layers of the multilayer stack;

(c) forming a conformal second mask on one or more sidewalls of the first mask;

(d) etching one or more layers of the multilayer stack ~~to the substrate surface~~ using the second mask to form an opening in the multilayer stack;

(e) filling the opening ~~formed in the multilayer stack~~ with one or more material layers; and

(f) removing the multilayer stack from the substrate leaving thereon a feature formed of the one or more material layers.

2. (Original) The method of claim 1 wherein step (b) further comprises:

(b1) forming a photoresist pattern on the multilayer stack;

(b2) transferring the photoresist pattern through one or more layers of the multilayer stack; and

(b3) removing the photoresist pattern from the multilayer stack.

3. (Original) The method of claim 1 wherein the first mask comprises at least one of a dielectric antireflective coating (DARC) and an amorphous carbon layer.

4. (Currently Amended) The method of claim 1 wherein step (c) further comprises;

(c1) depositing a second mask layer conformably on the first mask; and

(c2) etching portions of the second mask layer on horizontal surfaces of the substrate ~~leaving the second mask layer on one or more sidewalls of the first mask~~.

5. (Original) The method of claim 1 wherein the second mask comprises a material selected from the group consisting of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4).

6. (Original) The method of claim 1 wherein the one or more material layers filling the opening formed in the multilayer stack comprise polysilicon.

7. (Currently Amended) A method of fabricating a notch gate structure of a field effect transistor comprising:

(a) providing a substrate having a multilayer stack formed on a gate dielectric layer;

(b) forming a first mask ~~through~~ by patterning one or more layers of the multilayer stack;

(c) forming a conformal second mask on one or more sidewalls of the first mask;

(d) etching one or more layers of the multilayer stack to ~~the surface of~~ the gate dielectric layer using the second mask to form a notch gate opening in the multilayer stack;

(e) filling the notch gate opening ~~formed in the multilayer stack~~ with one or more material layers; and

(f) removing the multilayer stack from the substrate leaving thereon a a notch gate electrode formed on the gate dielectric layer.

8. (Original) The method of claim 7 wherein step (b) further comprises:

(b1) forming a photoresist pattern on the multilayer stack;

(b2) transferring the photoresist pattern through one or more layers of the multilayer stack; and

(b3) removing the photoresist pattern from the multilayer stack.

9. (Original) The method of claim 7 wherein the first mask comprises at least one of a dielectric antireflective coating (DARC) and an amorphous carbon layer.

10. (Currently Amended) The method of claim 7 wherein step (c) further comprises:

(c1) depositing a second mask layer conformably on the first mask; and

(c2) etching portions of the second mask layer on horizontal surfaces of the substrate ~~leaving the second mask layer on one or more sidewalls of the first mask~~.

11. (Original) The method of claim 7 wherein the second mask comprises a material selected from the group consisting of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4).

12. (Original) The method of claim 7 wherein the one or more material layers filling the notch gate opening formed in the multilayer stack comprise polysilicon.

13. (Currently Amended) A method of fabricating a field effect transistor, comprising:

(a) providing a substrate having a multilayer stack formed on a gate dielectric layer;

(b) forming a first mask ~~through~~ by patterning one or more layers of the multilayer stack;

(c) forming a conformal second mask on one or more sidewalls of the first mask;

(d) etching one or more layers of the multilayer stack to ~~the surface of~~ the gate dielectric layer using the second mask to form a notch gate opening in the multilayer stack;

(e) filling the notch gate opening ~~formed in the multilayer stack~~ with one or more material layers; and

(d) removing the multilayer stack from the substrate leaving thereon a a notch gate electrode formed on the gate dielectric layer.

14. (Original) The method of claim 13 wherein step (b) further comprises:

(b1) forming a photoresist pattern on the multilayer stack;

(b2) transferring the photoresist pattern through one or more layers of the multilayer stack; and

(b3) removing the photoresist pattern from the multilayer stack.

15. (Original) The method of claim 13 wherein the first mask comprises at least one of a dielectric antireflective coating (DARC) and an amorphous carbon layer.

16. (Currently Amended) The method of claim 13 wherein step (c) further comprises:

(c1) depositing a second mask layer conformably on the first mask; and

(c2) etching portions of the second mask layer on horizontal surfaces of the substrate ~~leaving the second mask layer on one or more sidewalls of the first mask~~.

17. (Original) The method of claim 13 wherein the second mask comprises a material selected from the group consisting of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4).

18. (Original) The method of claim 13 wherein the one or more material layers filling the notch gate opening formed in the multilayer stack comprise polysilicon.